

<b>Notice of Allowability</b>	Application No.	Applicant(s)
	10/517,534	TANAKA ET AL. <i>RW</i>
	Examiner	Art Unit
	Gary L. Laxton	2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to the application filed 12/13/2004.
2.  The allowed claim(s) is/are 1-8.
3.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All b)  Some\* c)  None of the:
    1.  Certified copies of the priority documents have been received.
    2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5.  CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 111405.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

#### Attachment(s)

1.  Notice of References Cited (PTO-892)
2.  Notice of Draftsperson's Patent Drawing Review (PTO-948)
3.  Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date 12/13/04
4.  Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5.  Notice of Informal Patent Application (PTO-152)
6.  Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7.  Examiner's Amendment/Comment
8.  Examiner's Statement of Reasons for Allowance
9.  Other Approved Drawing Corrections

*G.L.L.*  
 Gary L. Laxton  
 Primary Examiner  
 Art Unit: 2838  
*11/14/05*

## DETAILED ACTION

### EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

The following changes to the drawings have been approved by the examiner:  
Please label Figure 4 as "Prior Art".

2. Claims 1-8 are allowed.
3. The following is an examiner's statement of reasons for allowance:

Claims 1 and 2; prior art fails to disclose or suggest, inter alia, a PWM inverter control apparatus in which four switching units are connected in series for each phase, comprising: a current detecting circuit for detecting a current value of an output current; and a controller for outputting a zero vector to be started from a state in which all phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value measured by the current detecting circuit is equal to or greater than a first

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reference value and has a lower level than a level of a second reference value which is higher than a level of the first reference value, carrying out a base block operation for bringing all of the switching units into an OFF state after outputting the zero vector when the current value is equal to or greater than the second reference value and has a lower level than a level of a third reference value which is higher than the level of the second reference value, and executing an emergency stop when the current value is equal to or greater than the third reference value.

Claims 3 and 4; prior art fails to disclose or suggest, inter alia, a PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level; comprising: a current detecting circuit for detecting a current value of an output current; and a controller for outputting such a zero vector as to bring a state in which all of phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus level of the DC bus voltage and then carrying out a base block operation for bringing all of the switching units into an OFF state when the current value measured by the current detecting circuit is equal to or greater than a preset reference value, and for outputting such a zero vector as to bring all of the phases into the state and then performing a reset to a normal run when the current value is smaller than the reference value.

Claims 5 and 6; prior art fails to disclose or suggest, inter alia, a PWM inverter control method for controlling a PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising the steps of: detecting a current value of an output

current outputting a zero vector to be started from a state in which all phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value is equal to or greater than a first reference value which is preset and has a lower level than a level of a second reference value which is higher than a level of the first reference value; carrying out a base block operation for bringing all of the switching units into an OFF state after outputting the zero vector when the current value is equal to or greater than the second reference value and has a lower level than a level of a third reference value which is higher than the level of the second reference value; and executing an emergency stop when the current value is equal to or greater than the third reference value.

Claims 7 and 8; prior art fails to disclose or suggest, inter alia, a PWM inverter control method for controlling a PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising the steps of: detecting a current value of an output current; outputting such a zero vector as to bring a state in which all of phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value is equal to or greater than a preset reference value carrying out a base block operation for bringing all of the switching units into an OFF state after outputting the zero vector; and outputting such a zero vector as to bring all of the phases into the state and then performing a reset to a normal run when the current value is smaller than the reference value.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,795,323 Tanaka et al disclose a three level neutral point clamping PWM inverter; US 6,490,185 Yamanaka et al disclose controlling a neutral point potential of a neutral point clamping type inverter; US 5,361,196 Tanamachi et al disclose a power converter for converting a DC voltage into AC phase voltage.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Easthom Karl can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

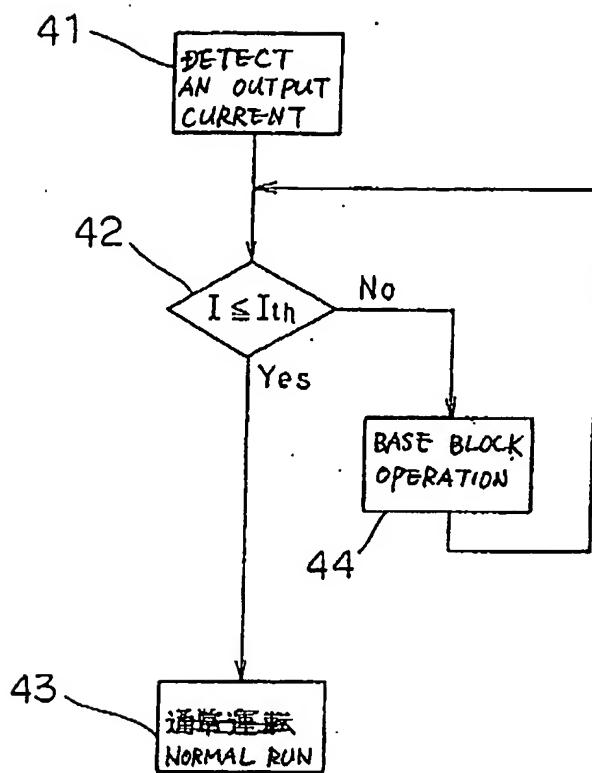
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Gary L. Laxton  
Primary Examiner  
Art Unit 2838

10/517534

FIG. 4 Prior Art



Prior Art

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11/4/05